Transmitter for an optical communication signal

The present invention relates to a transmitter for an optical RZ-DPSK communication signal. Such transmitters are used for transmission of communication signals at a high data rate on optical fibres. Optical transmitters for generating phase shift keyed signals generally comprise a laser for generating a narrow-band optical carrier and a modulator which receives the optical carrier from the laser and keys phase shifts on it based on a communication signal applied to it, in which information is encoded. The intensity of the carrier after its passage through the phase modulator is not modified by the modulation. An improvement of transmission quality, i.e. an improvement of the error rate and/or an increased range of the transmission with unchanged signal power can be achieved by imposing an RZ envelope onto such a signal, so that the symbols of the transmitted signal are separated from each other by a time interval in which the intensity of the transmitted signal becomes zero.

Prior art optical transmitters for a phase shift keyed RZ signal generally have the structure shown schematically in Fig. 1A. A laser 1 acts as a source for a carrier wave of constant power which is led through a phase-modulator 2 where phase shifts are keyed on it which correspond to information bits of a binary, usually electric communication signal DATA supplied to the phase modulator. The phase modulator 2 comprises a waveguide section from a bi-refringent material such as lithium niobate, the index of refraction of which varies under the influence of an electrode supplied with the electric communication signal DATA, and which can therefore assume two different levels of optical path length according to the level of the communication signal applied to it. The output signal M of the phase modulator has a constant power and is formed of a series of sections that may take two different values of the phase shift with respect to the carrier wave provided by laser 1, represented in the diagram of the signal M in Fig. 1A as hatched and unhatched sections, respectively. The different phase shifts correspond to diametrically opposed points in a constellation diagram shown in Fig. 1A. The transition between two sections of different phase is not instantaneous, but requires a short time interval in

which the phase of the output signal M of the modulator 2 changes continuously. I.e. in these times the state of the modulated signal M moves in the constellation diagram on a unit circle on which the two phase states corresponding to a symbol are located.

In order to suppress transition times of undetermined phase in signal M, the phase modulator 2 has an intensity modulator 3 connected to its output, which is supplied with a clock signal CLK, the frequency of which corresponds to the bit frequency of the communication signal data. The intensity modulator 3 provides a transmission signal T to be output on a waveguide in the form of a series of impulses, which are separated by time intervals with zero intensity and which can have two phase states with phases shifted by 180°.

In another known embodiment of an optical transmitter for a RZ-DPSK communication signal, the phase modulator 2 is replaced by an interferometer 4, in which at least one of its two arms has an optical path length that can be modified by the communication signal S. The output signal of the interferometer obtained by superimposing the partial signals transmitted on the two arms of the interferometer can assume different amplitudes according to the amount of the path length difference between the two arms, but it has only two possible phase values at all times, including transition phases between two symbols. The output signal of the interferometer 4 therefore has no constant envelope, but at each change of phase, the power of the modulated signal M goes through a minimum. In order to form an RZ signal from the output signal of the interferometer 4, it is conventional to lead the latter through an intensity modulator 3 which is supplied with the clock CLK of the communication signal DATA, just like the phase modulator 2 in Fig. 1A.

The two known designs of a RZ-DPSK transmitter therefore require two optical modulators, which are expensive and require a lot of space on a circuit board.

The object of the present invention is to provide a transmitter for an optical RZ-DPSK communication signal, which is economic in manufacture and requires little space on a circuit board.

The object is achieved by a transmitter having the features of claim 1.

The electro-optical intensity modulator according to the present invention must comprise at least one element, the optical path length of which is adapted to be modified by the driver signal, in order to be able to generate not only a change of intensity at constant phase of the optical carrier modulated with the communication signal, but also a zero-transition of the intensity accompanied by a phase reversal. Such an electro-optical modulator may be formed in a manner known as such as an interferometer in which at least one arm has an optical path length adapted to be controlled by the driver signal, but it is also conceivable to use a Faraday rotator to which the driver signal is applied, in combination with a subsequent linear polarizer.

In order to simplify the restoration, at a receiver side, of the communication signal from the output signal provided by the transmitter, the driver circuit of the transmitter advantageously comprises a difference circuit, which supplies a signal, referred to in the following as a pre-coded signal, which is representative of the difference between two subsequent bits of the electrical communication signal, and from which the driver signal applied to the intensity modulator is derived.

This difference circuit may simply be formed by a XOR-gate and a flip-flop.

The signal processing circuit may simply and conveniently be formed with four pairs of switches, each of which has a first and a second main port and a control port, wherein in each pair the first main ports of the switches are connected to each other and the control ports of the switches are supplied with mutually inverse input signals, wherein in a first and a second pair the second main ports are connected to two outputs of the driver circuit, and in a third and fourth pair, one of the two main ports is connected to one of the two outputs and the other second main port is connected to a first main port of the first and second pair, respectively. In such a switch array, the input signal of the first and second switch pairs may be a clock signal, and the input signal of the third and fourth switch pairs can be the pre-coded signal; conversely, the input signal of the first and second switch pairs may be the pre-coded signal, and the input signal of the third and fourth switch pairs may be a clock signal.

In order to achieve an optimum range of the communication signal generated by the transmitter and/or an optimum signal-noise-ratio at a receiver of this communication signal, it is desirable to have means for varying the duty cycle of the communication signal, which enable to optimise the duty cycle for given application. Such means may e.g. be formed by a mono-flop, the dwell time of which in the instable state is controllable.

Further features and advantages of the invention will become apparent by way of example from the subsequent description of embodiments referring to the appended drawings.

Fig. 1A and 1B, already discussed, are block diagrams of conventional RZ-DPSK transmitters and constellation diagrams thereof;

Fig. 2 is a block diagram of a transmitter according to the invention;

Fig. 3 shows schematically the structure of the interferometer of Fig. 2;

Fig. 4 is an exemplary circuit diagram of the driver circuit of Fig. 2;

Fig. 5 is an alternative circuit diagram of the driver circuit of Fig. 2; and

Fig. 6 is a block diagram of a receiver that is complementary to the transmitter of Fig. 2.

The optical transmitter of the invention shown in Fig. 2 comprises a driver circuit 6, which generates from an arriving electrical two-level communication signal DATA a pre-coded signal, the bits of which correspond to the difference between two subsequent bits of the communication signal DATA. By inserting time intervals with zero-level between the bits of the pre-coded signal D, a RZ-pre-coded signal is obtained, which is output from driver circuit 6 as a driver signal T to modulation input of an interferometer 4. An optical input of the interferometer 4 has a laser 1 connected to it which forms a source for a monochromatic optical carrier wave of constant power, on which the driver signal T is to be modulated.

Fig. 3 schematically shows the structure of an interferometer 4 of the Mach-Zehnder type. Two parallel waveguide branches 7, 8 connect the optical input 9 to an optical output 10. Each branch 7, 8 contains a Pockels cell 11, 12 in the form of an optical waveguide section made of a material such as lithium niobate, the index of refraction of which is variable for the polarization of the carrier wave supplied to optical input 9 under the influence of an electrical field that is generated by a voltage applied to electrodes 13. One of the two electrodes 13 of each Pockels cell is grounded, and the other is supplied with a DC voltage BIAS, which is selected so that the optical path length of the two branches 7, 8 differ by $\lambda/2$, wherein λ is the wavelength of the carrier provided by laser 1, and it is connected in a DC-uncoupled way to one of two conductors 14a, 14b that form a symmetric input for the driver signal T. The amplitude of the impulses of the driver signal T is selected such that the impulses cause a change of the optical path length of $\lambda/2$ in the Pockels cell 11, 12 to which they are applied. When the driver signal T has zero-level, the components of the carrier transmitted on the different branches 7, 8 interfere destructively at output 10, so that no optical power is transmitted. If an impulse of the driver signal T is present, the two components interfere constructively, a transmission signal X is provided at output 10 which assumes opposite phases, depending on which one of the two conductors 14a, 14b has the impulse applied to it.

An example for a structure of the driver circuit 6 is shown in Fig. 4. The communication signal DATA, which is initially assumed to be asymmetric, is applied to an input of a XOR-gate 17. Symmetric outputs of the XOR-gate 17 are connected to symmetric inputs D, $\overline{D}$ of a D flip-flop 18. Clock inputs C, $\overline{C}$ are connected to a symmetric clock signal CLK. The D flip-flop 18 has symmetric data outputs Q, $\overline{Q}$, the inverting output of which is fed back to the second input of the XOR-gate 17. Thus, the XOR-gate forms the (unsigned) difference between a present bit of the communication signal DATA and a bit which is stored in the D flip-flop 18 and is output at the output port Q thereof. The bit value output at output port Q is therefore always zero during a bit period, if in the previous bit period the bit at output port Q and the bit of the communication signal DATA were different, and it is one, if they were equal.

Data and clock output ports Q, $\bar{Q}$, C, $\bar{C}$ of the D flip-flop 18 are connected to a network of four pairs of transistors T1 to T8. The emitters of each pair are directly connected to each other. The bases of the transistors T1, T2 of the first pair are connected to the output ports $\bar{Q}$, Q, respectively, of the D flip-flop 18, just like those of transistors T3, T4 of the second pair. Similarly, the bases of transistors T5, T7 and T8, T6 of the third and fourth pairs, respectively, are connected to the clock signal C and the inverted clock signal $\bar{C}$, respectively. The collectors of transistors T5, T6 are connected to the first one of the conductors 14 that form the output of the driver circuit, and to ground via a resistor R1; similarly, the collectors of transistors T8, T7 are connected to the second conductor 14, and to ground via a resistor R2. The emitters of the fourth pair T6, T8 are connected to the collector of T2, those of the third pair T5, T7 to the collector of T3. The emitters of the first and second pairs are connected to a supply voltage via transistors T9, T10 that are open during transmission operation, and resistors R9, R10, respectively.

The switch network can have four different input states, namely Q=C=0; Q=0, C=1; Q=1, C=0 and Q=C=1. In the first of these states, the transistors T1, T9, T5, T3, T10 are open, and both conductors 14a, 14b are connected via these transistors and the resistors R9, R10 to the supply voltage, so that they are at the same level, which corresponds to a symmetric output signal of zero. In the state Q=0, C=1, the transistors T1, T9, T7, T3, T10 are open, so that the conductor 14a is at the supply voltage. Simultaneously, the transistors T6, T5, T4 are blocking, so that the conductor 14b is grounded by R2. In the state Q=1, C=0, both conductors 14a, 14b are connected to the supply voltage via transistors T8, T2, T9 and T4, T10, respectively, so that, again, the output signal is zero. In the state Q=C=1, the transistors T6, T2, T9 and T4, T10, respectively, are open, so that the conductor 14b is at the supply voltage, whereas T8, T1 and T3 are blocking, so that the conductor 14a is grounded. As can be readily seen, the network of transistors T1 to T10 always provides a zero-level when the clock signal is C=0; and if the clock signal is C=1, an impulse appears either on conductor 14a or 14b, according to the value of the data signal Q. Thus, the driver signal T is obtained. The interferometer 4 driven by this driver signal thus provides the transmission signal X schematically shown in Fig. 2 in the form of an impulse train, the impulses of which are separated by time intervals with a signal intensity of zero, and in

which the phase of the carrier may take two different values, represented in the Figure by the impulses being hatched or not hatched.

According to an advanced embodiment, a mono-flop 19 may be inserted in the clock signal lines Q, $\bar{Q}$ before or, as indicated in the Figure by a dashed rectangle, behind the flip-flop 18, the dwell time of which in the instable state is controllable and shorter than the period of the clock signal. By such a mono-flop acting symmetrically on the signals Q, $\bar{Q}$, the duty cycle of the transmission signal, i.e. the ratio between the duration of the impulses and that of the period of the transmission signal may be controlled.

In order to guarantee voltage levels of the driver signal T that provide the required delay of $\lambda/2$ at the Pockels cells 11, 12, an amplifier 15 may be inserted between the driver circuit 6 and the interferometer 4, as shown in Fig. 2.

Fig. 5 shows a second example of a driver circuit for a transmitter according to the invention. The components 17, 18, 19, T9, T10, R1, R2, R9, R10 are identical to those of Fig. 4 in arrangement and function, and are not described anew. Data and clock output ports Q, $\bar{Q}$, C, $\bar{C}$ of D flip-flop 18 are connected to a network of four pairs of transistors T1 to T8. The emitters of each pair T1, T2; T3, T4; T5, T7 and T6, T8, respectively, are directly connected to each other. The bases of the transistors T1, T2 of the first pair are connected to the clock signal C, $\bar{C}$, respectively. Similarly, the bases of transistors T3, T4; T5, T7 and T8, T6 of the second, third and fourth pairs, respectively, are connected to the output Q, $\bar{Q}$, respectively, of D flip-flop 18. The collectors of transistors T4, T5, T6 are connected to a first one of conductors 14 that form the output of the driver circuit, and to ground via a resistor R1; similarly, the collectors of transistors T3, T8, T7 are connected to the second conductor 14, and to ground via a resistor R2. The emitters of the pair T2, T6, T8 are connected to the collector of T2, those of pair T5, T7 to the collector of T1 and those of pair T3, T4 to the supply voltage via transistor T10 and resistor R10. The emitters of the first pair T1, T2 are connected to the supply voltage via transistor T9 and resistor R9. In transmission operation, both transistors T9, T10 are open.

In the first of the four input states Q=C=0; Q=0, C=1; Q=1, C=0 and Q=C=1 of the switch network, the transistors T1, T3, T5, T8 are open, and the two conductors 14a, 14b are connected via these transistors T9, T10, R9 and R10 to the supply voltage, so that a zero output signal is generated. In the state Q=0, C=1, the transistors T2, T3, T5, T8 are open, so that the conductor 14a is at the supply voltage. Simultaneously, the transistors T1, T4, T6, T7 are blocking, so that the conductor 14b is grounded by R2. In the state Q=1, C=0, T1, T4, T6, T7 are open, so that both conductors 14a, 14b are at the supply voltage and again, a zero output signal is generated. In the state Q=C=1, the transistors T2, T4, T6, T7 are open, so that the conductor 14b is at the supply voltage, and the conductor 14a is grounded. The behaviour of the driver circuit of Fig. 5 does not differ from that of the circuit of Fig. 4.

In a receiver, as shown schematically in Fig. 6, the communication signal DATA is restored from the transmitter signal X. To this end, the latter is distributed onto two fibres 21a, 21b at a directional coupler 20, and the signal in fibre 21b is delayed with respect to that of fibre 21a by one bit period. Depending on whether the phases of two subsequent impulses of the received signal X are equal or opposite, constructive or destructive interference occurs at a photo detector 23, downstream of the second directional coupler 22. The photo detector 23 provides a pulsed output signal, the levels of which are equal to those of the signal DATA.